Logic level TOPFET

PIP3119-P

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in **TOPFET2** technology assembled in a 3 pin plastic package.

APPLICATIONS

General purpose switch for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		20	A
P_D	Total power dissipation		90	W
T_j	Continuous junction temperature		150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance		28	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

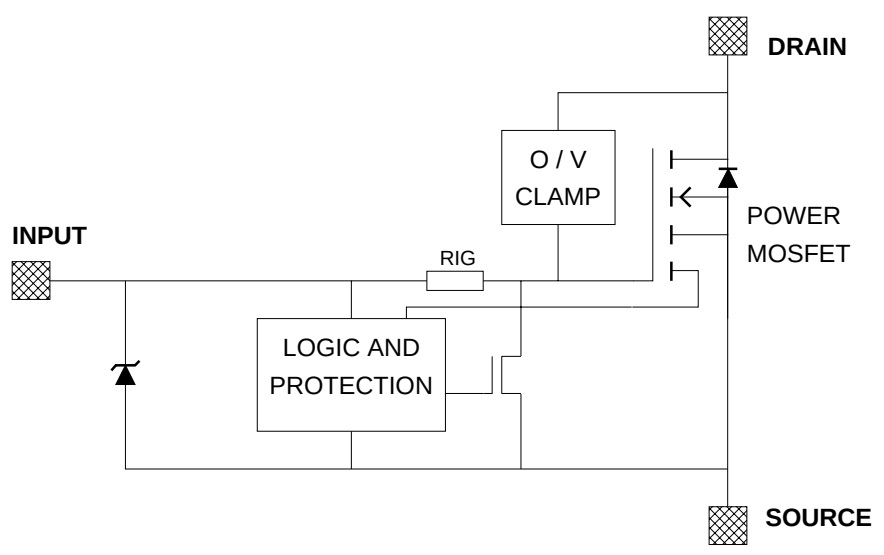
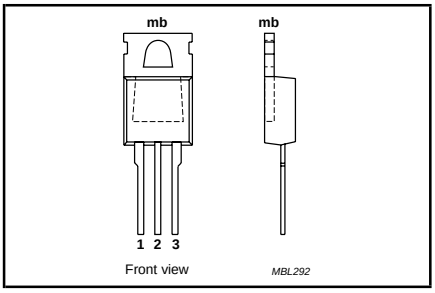


Fig.1. Elements of the TOPFET.

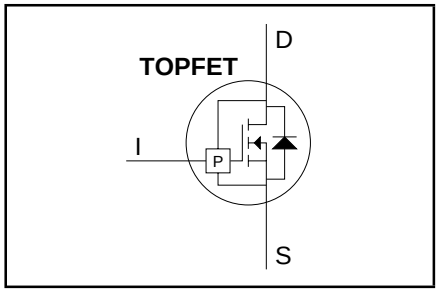
PINNING - SOT78B

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]		-	50	V
I_D	Continuous drain current	V_{IS} = 5 V; T_{mb} = 25˚C	-	self - limited	A
I_D	Continuous drain current	V_{IS} = 5 V; $T_{mb} \leq$ 121˚C	-	20	A
I_I	Continuous input current		-5	5	mA
I_{IRM}	Repetitive peak input current	$\delta \leq 0.1$, tp = 300 µs	-50	50	mA
P_D	Total power dissipation	$T_{mb} \leq$ 25˚C	-	90	W
T_{stg}	Storage temperature		-55	175	˚C
T_j	Continuous junction temperature[2]	normal operation	-	150	˚C
T_{sold}	Lead temperature	during soldering	-	260	˚C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Inductive load turn-off	I_{DM} = 20 A; $V_{DD} \leq$ 20 V			
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq$ 25˚C	-	350	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq$ 95˚C; f = 250 Hz	-	45	mJ

OVERLOAD PROTECTION LIMITING VALUE

With an adequate protection supply provided via the input pin, TOPFET can protect itself from two types of overload - overtemperature and short circuit load.

SYMBOL	PARAMETER	REQUIRED CONDITION	MIN.	MAX.	UNIT
V_{DS}	Drain source voltage[3]	4 V $\leq V_{IS} \leq$ 5.5 V	0	35	V

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.25	1.39	K/W

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 All control logic and protection functions are disabled during conduction of the source drain diode.

OUTPUT CHARACTERISTICS

Limits are for -40˚C ≤ T_{mb} ≤ 150˚C; typicals are for T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Off-state	V_{IS} = 0 V				
$V_{(CL)DSS}$	Drain-source clamping voltage	I_D = 10 mA	50	-	-	V
		I_{DM} = 4 A; t_p ≤ 300 µs; δ ≤ 0.01	50	60	70	V
I_{DSS}	Drain source leakage current	V_{DS} = 40 V	-	-	100	µA
		T_{mb} = 25˚C	-	0.1	10	µA
	On-state	V_{IS} ≥ 4.4 V; t_p ≤ 300 µs; δ ≤ 0.01				
$R_{DS(ON)}$	Drain-source resistance	I_{DM} = 10 A	-	-	52	mΩ
		T_{mb} = 25˚C	-	22	28	mΩ

OVERLOAD CHARACTERISTICS

V_{IS} = 5 V; T_{mb} = 25˚C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load					
I_D	Drain current limiting	V_{DS} = 13 V	28.5	43	57	A
		4.4 V ≤ V_{IS} ≤ 5.5 V; -40˚C ≤ T_{mb} ≤ 150˚C	21	-	65	A
	Overload protection					
$P_{D(TO)}$	Overload power threshold	device trips if P_D > $P_{D(TO)}$	75	185	250	W
T_{DSC}	Characteristic time	which determines trip time[1]	200	380	600	µs
	Overtemperature protection					
$T_{j(TO)}$	Threshold junction temperature[2]		150	170	-	˚C

1 Trip time $t_{d\,sc}$ varies with overload dissipation P_D according to the formula $t_{d\,sc} \approx T_{DSC} / \ln[P_D / P_{D(TO)}]$.

2 This is independent of the dV/dt of input voltage V_{IS}.

INPUT CHARACTERISTICS

The supply for the logic and overload protection is taken from the input.
Limits are for -40˚C ≤ T_{mb} ≤ 150˚C; typicals are for T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		0.6	-	2.4	V
			T_{mb} = 25˚C	1.1	1.6	2.1	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	220	400	µA
			V_{IS} = 4 V	80	195	330	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	200	400	650	µA
			V_{IS} = 3 V	130	250	430	µA
V_{ISR}	Protection reset voltage[1]	reset time t_r ≥ 100 µs		1.5	2	2.9	V
t_{lr}	Latch reset time	V_{IS1} = 5 V, V_{IS2} < 1 V		10	40	100	µs
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		5.5	-	8.5	V
R_{IG}	Input series resistance[2] to gate of power MOSFET		T_{mb} = 25˚C	-	33	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25˚C; V_{DD} = 13 V; resistive load R_L = 4 Ω. Refer to waveform figure and test circuit.

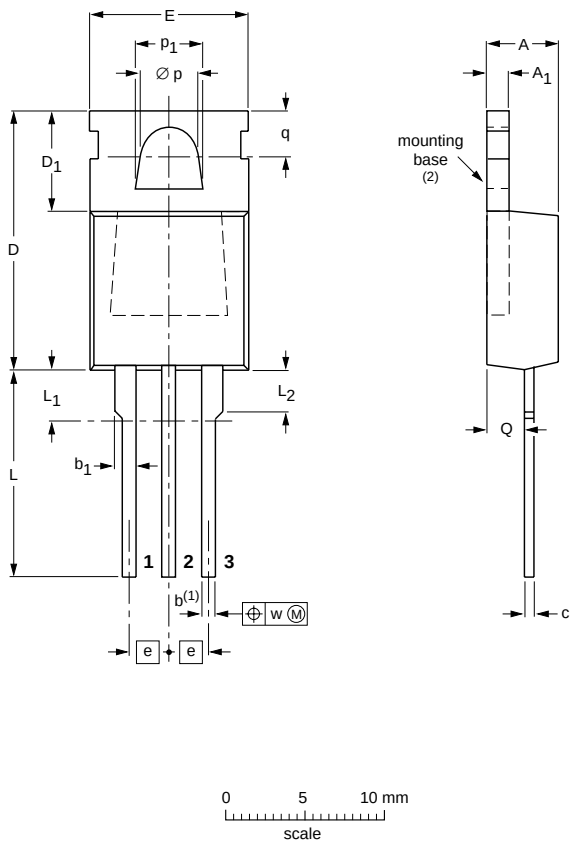
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	V_{IS} = 5 V	-	25	50	µs
t_r	Rise time		-	50	100	µs
$t_{d\ off}$	Turn-off delay time	V_{IS} = 0 V	-	60	120	µs
t_f	Fall time		-	50	100	µs

1 The input voltage below which the overload protection circuits will be reset.

2 Not directly measureable from device terminals.

MECHANICAL DATA

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-leads **SOT78B**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	$b^{(1)}$	b_1	c	D	D_1	E	e	L	L_1	L_2 max.	∅ p	p_1	q	Q	w
mm	4.5 4.1	1.39 1.27	0.85 0.60	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	4.3 4.1	3.0 2.7	2.6 2.2	0.4

Notes

1. The positional accuracy of the terminals is controlled within zone L_1 max.
2. Mounting base configuration is not defined within the dimensions E and D

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78B						01-02-22

Fig.2. SOT78B (TO220AB) package[1], pin 2 connected to mounting base.

1 Refer to mounting instructions for SOT78 (TO220) envelopes. Epoxy meets UL94 V0 at 1/8". Net mass: 2 g

DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS[1]	**PRODUCT STATUS**[2]	**DEFINITIONS**
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in ordere to improve the design and supply the best possible product
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Limiting values		
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Application information		
Where application information is given, it is advisory and does not form part of the specification.		
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